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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,840	01/16/2004	Huilong Zhu	FIS920030237	1839

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,840	ZHU ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 23-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 23-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0104 & 0805*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 01/16/2004 through 09/22/2005.

Claims 1-15 and 23-28 are active in this application.

Claim(s) 16-22 have been cancelled. This cancellation has been made along with an election without traverse to prosecute the invention of Group II, claims 1-15, and 23-28, drawn to method of making semiconductor devices,

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 01/22/2004 and 08/23/2005. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Specification

3. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. The claim is objected to for the following reasons:

In claim12, the character "fomied" in line 1 should be changed to –formed--.

In claims 23-28, the phrases "semiconductor structure" should be changed to –method-- because their base claims are method claims, not device claims.

In addition, claims 23, 24, and 26-28 contain or repeat all limitations of claims 8, 9, and 12-14, respectively.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim(s) 1-4, and 7 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,420,766 to Brown et al.

Regarding claim 1, Brown discloses a method of fabricating a semiconductor structure, as shown in figs. 25-40, comprising the steps of:

forming a raised source region 2806 on a substrate 2500;

forming a raised drain region 2808 on the substrate 2500; and

forming a first silicon layer 3502 or 3802 over the raised source region 2806 and a second silicon layer 3502 or 3804 over the raised drain region 2808. See also col. 14, line 47 to col. 20, line 17.

Regarding claim 2, Brown discloses the method wherein the substrate includes a SiGe layer atop a buried oxide layer. See col. 20, lines 28-43.

Regarding claim 3, Brown discloses the method further comprising a step of forming a gate stack 2804 on the substrate 2500. See figs. 34-40.

Regarding claim 4, Brown discloses the method further comprising a step of forming a trench isolation 2402 surrounding the gate stack, source region and drain region. See fig. 25.

Regarding claim 7, Brown discloses the method wherein the first silicon layer 3802 is epitaxially formed silicon and the second silicon layer 3804 is epitaxially grown silicon. See col. 18, lines 14-48.

7. Claim(s) 1, 5-6, 8-15 and 23-28 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,214,679 to Murthy et al.

Regarding claim 1, Murthy discloses a method of fabricating a semiconductor structure, as shown in figs. 2-13, comprising the steps of:

forming a raised source and a raised regions 218 on a substrate 202; and

forming a first and a second silicon layers (by performing implantation illustrated by fig. 9, and col. 7, lines 15-26 over the raised source and the raised drain region. See also col. 3, line 9 to col. 8, line 62.

Regarding claim 5, Murthy discloses the method further comprising a step of forming a first silicide contact 236 on the first silicon layer. See figs. 11-13.

Regarding claim 6, Murthy discloses the method further comprising a step of forming a second silicide contact on the second silicon layer. See figs. 11-13.

Regarding claims 8 and 23, Murthy discloses the method wherein the raised drain region is comprised of a strained silicon layer 238 atop a SiGe layer 218. See figs. 12-13.

Regarding claims 9 and 24, Murthy discloses the method wherein the strained silicon layer is comprised of epitaxially grown silicon. See col. 7, line 27 to col. 8, line 62.

Regarding claim 10, Murthy discloses the method wherein the raised source region is comprised of a strained silicon layer atop a SiGe layer. See figs. 12-13.

Regarding claim 11, Murthy discloses the method wherein the strained silicon layer is comprised of epitaxially grown silicon. See col. 7, line 27 to col. 8, line 62.

Regarding claims 12 and 26, Murthy discloses the method wherein the first silicon layer formed over the raised source region and the second silicon layer over the raised drain region include cap portions 234 and sidewall portions, the method further comprising a step of forming sacrificial spacers 232 along the silicon sidewall portions. See col. 7, line 27 to col. 8, line 62.

Regarding claims 13, and 27, Murthy discloses the method further comprising steps of: forming a third silicon layer over the cap of the first silicon layer over the raised source region; and forming a fourth silicon layer over the cap of the second silicon layer over the raised drain region. These are inherent because the device needs contact plugs being formed above and connecting to the source/drain regions to provide accesses to the source/drain regions.

Regarding claims 14, and 28, Murthy discloses the method further comprising a step of removing the sacrificial spacers. See col. 8, lines 8-21.

Regarding claim 15, Murthy discloses the method wherein the step of removing the sacrificial spacers includes etching away the sacrificial spacers. See col. 8, lines 8-21.

Regarding claim 25, Murthy discloses the method wherein the raised source region and the raised drain region are comprised of a strained silicon layer 238 atop a SiGe layer 218. See figs. 12-13.

Conclusion

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
September 30, 2005